## AMENDMENTS TO THE CLAIMS

Claim 1 (original) A soft metal conductor for use in a semiconductor device comprising grains having grain sizes larger than 200 nm so as to provide a substantially scratch-free surface upon polishing in a subsequent chemical mechanical polishing step, said soft metal conductor being formed by at least one metal selected from the group consisting of Al, Cu and Ag.

Claim 2 (original) An electrically conducting soft metal structure for use in a semiconductor device comprising:

an uppermost layer consisting of grains having grain sizes not smaller than 200 nm, and

a second layer contiguous with and immediately adjacent to said uppermost layer consisting of grains having grain sizes not larger than about 20% of the thickness of said soft metal structure.

Claim 3 (original) An electrically conducting soft metal structure according to claim 2, wherein said uppermost layer having a thickness sufficiently large to provide a substantially scratch-free and erosion-free surface upon polishing in a chemical mechanical polishing method.

Claim 4 (original) An electrically conducting soft metal structure according to claim 2, wherein said structure being made of a metal selected from the group consisting of aluminum, copper, silver, ternary and binary alloys of aluminum, copper, silver and any other low resistance metal.

Claim 5 (original) An electrically conducting soft metal structure according to claim 2, wherein said structure being a member selected from the group consisting of a via, an interconnect and a line.

Claim 6 (original) An electrically conducting soft metal structure according to claim 2, wherein said uppermost layer having grains of metal not less than 200 nm in grain size and a thickness of at least 100 nm.

Claim 7 (original) An electrically conducting soft metal structure according to claim 2, wherein said uppermost layer having grains of metal not less than 200 nm in grain size and said second layer having grains of metal not more than 100 nm in grain size.

Claim 8 (original) An electrically conducting soft metal structure according to claim 2, wherein said second layer having grains of metal not more than 100 nm in grain size and a thickness of not less than 600 nm.

Claim 9 (original) An electrically conducting soft metal structure according to claim 2 further comprising a bottom layer contiguous with and immediately adjacent to said second layer, said bottom layer consisting of grain of metal not less than 200 nm in grain size.

Claim 10 (original) A soft metal conductor for use in a semiconductor device comprising:

a first soft metal layer;

a Ti layer of less than 30 nm thickness on top of said first metal layer;

a second soft metal layer on top of said Ti layer having in its uppermost surface metal grains of grain sizes not smaller than about 20% of the thickness of said second metal layer, said first soft metal layer and said second soft metal layer are formed by at least one metal selected from the group consisting of Al, Cu and Ag; and

whereby said Ti layer sandwiched between two soft metal layers is converted to $TiAl_3$ upon annealing at a temperature higher than room temperature such that diffusion of atoms of said metal through said $Ti\ Al_3$ film occurs upon the passage of an electrical current therethrough and thus improving the electromigration resistance of said soft metal conductor.

Claim 11 (original) A soft metal structure according to claim 10, wherein said first soft metal is formed by a member selected from the group consisting Al, Cu, Ag, CuAg, CuAl, AgAl and CuAgAl.

Claim 12 (original) A soft metal conductor according to claim 10, wherein said Ti layer further comprising composite layers of Ti and Ti alloys including Ti/TiN.

Claim 13 (original) A soft metal conductor according to claim 10, wherein said Ti layer is situated at the bottom of a via having portions of said layer in extremely small thickness or portions of said layer in voids so as to allow the existence of a continuous phase of said metal material or diffusion of said metal atoms across a $TiAl_3$ layer subsequently formed and a resulting improvement in the electromigration resistance of said soft metal conductor.

Claim 14 (original) A soft metal conductor according to claim 10 further comprising an annealing step at a predetermined temperature and for a predetermined length of time sufficient to convert said Ti layer to $TiAl_3$ when said soft metal used in forming said first soft metal layer and said second soft metal layer is Al or AlCu.

Claim 15 (original) A soft metal conductor according to claim 14, wherein said predetermined temperature is not less than 300 °C. and said predetermined length of time is not less than 10 min.

Claim 16 (original) A soft metal conductor according to claim 14, wherein said predetermined temperature is 400 °C. and said predetermined length of time is 30 min.

Claim 17 (previously presented) A semiconductor structure, comprising:

a plated multigrained soft metal conductor having a polished upper surface, said plated multigrained soft metal conductor containing at least some individual grains having a size of at least 200 nm, wherein said soft metal conductor is formed over an underlying semiconductor layer, said underlying semiconductor layer having at least one semiconductor device therein.

Claim 18 (previously presented) The structure according to claim 17 wherein said semiconductor layer comprises logic and memory devices on a single chip.

Claim 19 (previously presented) The structure according to claim 17 wherein said soft metal conductor is selected from the group consisting of Cu, Al, Ag and alloys thereof.

Claim 20 (previously presented) The structure of claim 17 wherein said plated multigrained soft metal conductor is an electroplated multigrained soft metal conductor.

Claim 21 (previously presented) The structure of claim 17 wherein said plated multigrained soft metal conductor is an electrolessly plated multigrained soft metal conductor.

Claim 22 (currently amended) A semiconductor structure comprising a conductive metal line, said metal line interconnecting devices in a semiconductor chip, said metal line having low electrical resistance and being comprised of a plated soft metal, said plated soft metal having an upper surface, said upper surface being a polished surface, said metal line comprised of grains, said upper surface provided with a wear resistance in accordance with a size of said grains ~~sufficiently large~~ so as to prevent substantial scratching of said upper surface during polishing.

Claim 23 (previously presented) The structure according to claim 22 wherein said soft metal is selected from the group consisting of Cu, Al, Ag and alloys thereof.

Claim 24 (previously presented) The structure according to claim 22 wherein said soft metal is selected form the group consisting of Cu and alloys thereof.

Claim 25 (previously presented) The structure according to claim 22 wherein said plated soft metal is an electroplated soft metal.

Claim 26 (previously presented) The structure according to claim 22 wherein said plated soft metal is an electrolessly plated soft metal.

Claim 27 (previously presented) The structure according to claim 22 wherein said conductive metal line is formed using a damascene process.

Claim 28 (previously presented) The structure according to claim 22 wherein said conductive metal line is formed using a dual damascene process.

Claim 29 (currently amended) An interconnecting structure of a semiconductor chip, the chip including a layer of semiconducting material having devices therein, the interconnecting structure comprising:

a first electrically conductive layer electrically contacting at least one device;

a second electrically conductive layer overlying and contacting said first electrically conductive layer, said second electrically conductive layer being formed in an insulator overlying said first electrically conductive layer, said second conductive layer being a plated soft metal having an upper surface, said upper surface being a polished surface, said second electrically conductive layer comprised of grains, said upper surface provided with a wear resistance in accordance with a size of said grains ~~sufficiently large~~ so as to prevent substantial scratching of said upper surface during polishing.

Claim 30 (previously presented) The structure according to claim 29 wherein at least a portion of said individual grains comprising said second conductive layer have a size of at least about 200 nm.

Claim 31 (previously presented) The structure according to claim 29 wherein said plated soft metal is selected from the group consisting of Cu, Al, Ag and alloys thereof.

Claim 32 (previously presented) The structure according to claim 29 wherein said plated soft metal is selected from the group consisting of Cu and alloys thereof.

Claim 33 (previously presented) A semiconductor structure, comprising:

a semiconductor chip having devices therein; and

a plated soft metal layer interconnecting said devices, said soft metal selected from the group consisting of Cu and alloys thereof, said soft metal layer having a polished substantially scratch free surface.

Claim 34 (previously presented) The semiconductor structure according to claim 33 wherein said soft metal layer is a damascene layer.

Claim 35 (previously presented) An electrically conducting soft metal structure according to claim 2 wherein said second layer is formed by at least one metal selected from the group consisting of Cu and alloys of Cu with at least one member selected from the group consisting of C, B, N, Group IIIA elements, Group IVA elements and Group VA elements.

Claim 36 (previously presented) The soft metal conductor according to claim 1 being a plated soft metal conductor.

Claim 37 (previously presented) The soft metal conductor according to claim 36 being an electroplated or electrolessly plated metal conductor.